REMARKS

Claims 1-30 are pending in the application. Claims 27-30 are withdrawn from consideration. Claims 1-26 are rejected.

During a telephone conservation with Eugene Kim on 04/05/2006, a provisional election was made with traverse to prosecute the invention of group a, claims 1-26. Applicants affirm the election of group a, without traverse.

Applicants have amended the Specification as indicated to correct references to U.S. Patent Applications and U.S. Patents which are incorporated into the Specification. Applicants do not add new matter with these amendments to the Specification.

Applicants respectfully request reconsideration of the present application in view of the amendments above and the remarks set forth below.

REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1, 4-9, 12, 14-15, 17-21, and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,999,734 to Willis et al. (hereinafter "Willis"). Applicants respectfully traverse these rejections.

Amended claim 1 recites in part, "a software extensible device configured to provide additional new instructions to a set of standard instructions for the processing element wherein the new instructions can be programmed by software". (Supported in paragraph 33 of the Specification.) In rejecting claim 1, the Office Action states that Willis has taught in part, "a software extensible device *[re-configurable logic block; Fig. 1, component 9]* configured to provide additional instructions to a set of standard instructions for the processing element *[column 6, lines 1-8]*". Applicants traverse this statement.

Willis teaches a distributed, compiler-oriented database to support "parallel database clients such as a source code analyzer, an elaborator, an optimizer, mapping and scheduling, code generation, linking/loading, execution/simulation, debugging, profiling, user interface and a file interface." (Abstract.) In this context, Willis discloses re-configurable logic blocks in which "[o]ne or more instruction set encodings (commonly known as 'op-codes'[)] may be reserved for functional implemented [sic] by an optional coprocessor, interconnect, arbiter and re-configurable logic block." (col 6, line 4-8.) Thus, the op-codes for the re-configurable logic block are reserved from the instruction set encodings of the processor and are to be selected from the op-codes designed for the processor. For example, if the processor in Willis is configured to execute 100 op-codes, 10 of those op-codes may be reserved for functional implementation by the re-configurable logic block. Thus, the re-configurable logic block of Willis is not configured to accept additional new instructions and may implement only reserved instructions.

In contrast, the software extensible device of amended claim 1 provides additional new instructions. These additional new instructions are not reserved, as are the op-codes disclosed in Willis. The software extensible device of amended claim 1 provides several advantages over the re-configurable logic block of Willis. For example, the software extensible device may store and execute instructions beyond the hard-coded instruction set of the processing element. The ability to execute instructions beyond the hard-coded instruction set of the processor is absent from the re-configurable logic block of Willis. In addition, the new instructions of the software extensible device are not limited and can expanded in number as needed to execute an application, unlike the reserved number of op-codes in Willis. Furthermore, these new instructions may be programmed by software (supported in paragraph 33 of the Specification).

This programming capability enhances the ability of the software extensible device to adapt to a variety of processing applications.

Thus, Willis does not teach a software extensible device configured to provide additional new instructions to a set of standard instructions for the processing element wherein the new instructions can be programmed by software, as recited in amended claim 1. Therefore, amended claim 1 is allowable for at least the above reasons over Willis.

Furthermore, amended claim 1 recites, in part, "a communication interface configured to communicate with other processor nodes using different communication protocols based on whether or not a neighboring processor node comprises another software extensible device and whether the neighboring processor node is on a separate chip or on a same chip". (Supported in paragraphs 81-82 of the Specification). In rejecting claim 1, the Office Action states that Willis discloses in part, "a communication interface *[message interface, FIG. 1, component 10]* configured to communicate with the other processor nodes *[column 5, lines 4-8]"*.

Willis teaches communication between processors nodes using a message interface coupled to a message interconnect. Specifically, communication between processors in node 11 (FIG. 1, block 11, components 1 and 2) and processors in node 12 (FIG. 1, block 12, components 1 and 2) is via a message interface (FIG. 1, component 10) coupled to a message interconnect (FIG. 1, component 13). Willis further teaches that each re-configurable logic block communicates to the processors in its processor node via a shared memory interconnect, and to other processor nodes via the message interconnect, regardless of the physical or logical location of other processors and/or of the other re-configurable logic blocks. Thus, communication between multiple processor nodes in Willis is provided by a message interconnect.

In contrast, amended claim 1 recites, in part, a communication interface configured to communicate with other processor nodes using different communication protocols based on whether or not a neighboring processor node comprises another software extensible device. For example, in the case where the neighboring processor node is not a software extensible device, the processor node communicates with a neighboring processor node using a communication protocol such as standard input/output processing. In the case where the neighboring processor node is a software extensible device, the processor node communicates with a neighboring processor node using a different communication protocol using, for example, an array interface module specifically configured to communicate to the neighboring processor node. The ability to use different communication protocols based on the neighboring processor nodes is not taught or suggested in Willis. Rather, Willis teaches that communication between multiple processor nodes, regardless of the location of the processor nodes, is provided by a message interconnect.

Furthermore, Willis does not teach or suggest a different communication protocol for software extensible devices. For the reasons discussed above, the re-configurable logic blocks of Willis are not equivalent to software extensible devices, and thus Willis does not teach or suggest software extensible devices. Thus, Willis does not teach or suggest different communication protocols based on whether or not a neighboring processor node comprises another software extensible device, as recited in amended claim 1.

Moreover, amended claim 1 recites, in part, using different communication protocols based on whether the neighboring processor node is on a separate chip or on a same chip. There is no discussion in Willis about whether processor nodes are on the same or separate chips. Thus, Willis does not teach or suggest using different communication protocols based on whether or not a neighboring processor node comprises another software extensible device and

whether the neighboring processor node is on a separate chip or on a same chip, as recited in amended claim 1. Therefore, amended claim 1 is further allowable for at least the above reasons over Willis.

Claims 4-9, 12, 14-15, and 17 are dependent on claim 1 and are allowable for at least the same reasons as claim 1 over Willis.

Claim 18 has been amended to contain similar limitations as claim 1 and is allowable for at least the same reasons as claim 1 over Willis.

Claims 19, 20, 21, 24-25 are dependent on claim 18 and are allowable for at least the same reasons as claim 18 over Willis.

REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 2, 3, 10, 11, 13, 16, 22, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis. Applicants respectfully traverse these rejections.

Claims 2, 3, 10, 11, 13 and 16 are dependent on claim 1 and are allowable for at least the same reason as claim 1 over Willis. Claims 22 and 23 are dependent on claim 21, which is dependent on claim 18, and are allowable for at least the same reasons as claim 18 over Willis. Claim 26 is dependent on claim 18 and is allowable for at least the same reasons as claim 18 over Willis.

Furthermore, in rejecting claim 2, the Office Action states that "Willis has not explicitly taught that each one of the processor nodes is on a separate chip. The Examiner takes Official Notice that having each processor node on a separate chip is conventional and well-known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis to have each processor node on a separate chip since doing so would

reduce system cost." Applicants respectfully traverse the Examiner's taking Official Notice of this fact.

As claim 2 is dependent on claim 1, and as discussed above with reference to amended claim 1, having each processor node with a software extensible device on a separate chip is not conventional and well known. Further, having each processor node on a separate chip could feasibly increase systems costs by requiring additional interface circuitry to couple the multiple processor nodes. Additionally, Applicants find no teaching or suggestion in Willis for having each processor node on a separate chip. Applicants respectfully remind the Examiner that MPEP §2144.03 states

> It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well-known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art.

Therefore, Applicants request that the Examiner provide a citation to some reference work recognized as standard in the pertinent art that the elements of claim 2 were conventional and well-known at the time of the application, or withdraw the rejection of claim 2.

In rejecting claim 3, the Office Action states that "Willis has not explicitly taught that at least some of the processor nodes are on the same chip. However, the Examiner takes Official Notice that having some processor nodes on the same chip is conventional and well-known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis to have some of the processor nodes on the same chip since doing so would reduce the total space consumed by the system." Applicants respectfully traverse the Examiner's taking Official Notice of this fact.

As claim 3 is dependent on claim 1, and as discussed above with reference to amended claim 1, having at least some of the processor nodes with a software extensible device on the same chip is not conventional and well known. Further, because the total space consumed by the system may not be an important design parameter, given the ongoing miniaturization of the semiconductor processing components comprising the processor nodes, there may be no motivation to reduce the total space consumed by the system. For example, Applicants find no teaching or suggestion in Willis for having some of the processor nodes on the same chip to reduce the total space consumed by the system. Applicants request that the Examiner provide a citation to some reference work recognized as standard in the pertinent art that the elements of claim 3 were conventional and well-known at the time of the application, or withdraw the rejection of claim 3.

In rejecting claim 10, the Office Action states that "Willis has not explicitly taught that the communications interface is configured to perform time division multiplexing using the channels between the processor nodes. However, the Examiner takes Official Notice that communications interfaces configured to perform time division multiplexing using the channels between the processor nodes are conventional and well-known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that the communications interface is configured to perform time division multiplexing using the channels between the processor nodes since doing so allows a single transmission path to be shared by multiple signals." Applicants respectfully traverse the Examiner's taking Official Notice of this fact.

Because time division multiplexing is a technology conventionally applied to telecommunications, it may not be conventional and well-known in the field of computer

interfaces using channels between the processor nodes comprising software extensible devices. Further, Applicants find no teaching or suggestion in Willis to support time division multiplexing using channels between the processor nodes. Applicants request that the Examiner provide a citation to some reference work recognized as standard in the pertinent art that the elements of claim 10 were conventional and well-known at the time of the application, or withdraw the rejection of claim 10.

In rejecting claim 11, the Office Action states that "Willis has not explicitly taught that the communications interface is configured to perform spatial division multiplexing using the channels between the processor nodes. However, the Examiner takes Official Notice that communications interfaces configured to perform spatial division multiplexing using the channels between the processor nodes are conventional and well-known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that the communications interface is configured to perform spatial division multiplexing using the channels between the processor nodes since doing so increases data transmission speed." Applicants respectfully traverse the Examiner's taking Official Notice of this fact.

Because spatial division multiplexing is a technology conventionally applied to telecommunications, it may not be conventional and well-known in the field of computer interfaces using the channels between the processor nodes comprising software extensible devices. For example, Applicants find no teaching or suggestion in Willis to support spatial division multiplexing using channels between processor nodes. Applicants request that the Examiner provide a citation to some reference work recognized as standard in the pertinent art

that the elements of claim 11 were conventional and well-known at the time of the application, or withdraw the rejection of claim 11.

In rejecting claim 13, the Office Action states that "Willis has not explicitly taught that the communications interface comprises a processor network switch. However, the Examiner takes Official Notice that communications interfaces comprising a processor network switch are conventional and well-known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that the communications interface comprises a processor network switch since doing so advantageously allows the connection of multiple network segments." Applicants respectfully traverse the Examiner's taking Official Notice of this fact.

Because the processor nodes may comprise software extensible devices, the use of a network switch coupling such processor nodes may not be conventional and well-known. Furthermore, Applicants find no teaching or suggestion in Willis to support a communications interface comprising a processor network switch. Applicants request that the Examiner provide a citation to some reference work recognized as standard in the pertinent art that the elements of claim 13 were conventional and well-known at the time of the application, or withdraw the rejection of claim 13.

In rejecting claim 16, the Office Action states that "Willis has not explicitly taught that the communications interface comprises a multiplexer/demultiplexer. However, the Examiner takes Official Notice that communications interfaces comprising a multiplexer/demultiplexer are conventional and well-known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that the communications interfaces comprises a multiplexer/demultiplexer since doing so allows the combination of

multiple data streams into a single data stream that can be advantageously transmitted over a single transmission link." Applicants respectfully traverse the Examiner's taking Official Notice of this fact.

Because the multiplexer/demultiplexer is a part of the software extensible processor chip, as supported by paragraph 79 of the Specification, the use of a multiplexer/demultiplexer handling communications to a software extensible device may not be conventional and well known. Furthermore, Applicants find no teaching or suggestion in Willis to support a communications interface comprising a multiplexer/demultiplexer. Applicants request that the Examiner provide a citation to some reference work recognized as standard in the pertinent art that the elements of claim 16 were conventional and well-known at the time of the application, or withdraw the rejection of claim 16.

Claims 22 and 23 are allowable for at least the same reasons as claims 10 and 11, respectively.

In rejecting claim 26, the Office Action states that "Willis has not explicitly taught configuring one of the processor nodes to select between an interface module and a standard input/output interface based on a neighboring device. However, the Examiner takes Official Notice that configuring processor nodes to select between an interface module and a standard input/output interface based on a neighboring device is conventional and well-known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that processor node is configured to select between an interface module and a standard input/output interface based on a neighboring device since doing so would allow communication between the neighboring device and the processor node." Applicants respectfully traverse the Examiner's taking Official Notice of this fact.

As discussed with reference to amended claims 1 and 18 above, the ability of a processor node to select between an interface module and standard input/output interface based on a neighboring device, where the device may comprise a software extensible device, may not be conventional and well known. Furthermore, Applicants find no teaching or suggestion in Willis to support a both an interface module between neighboring processor nodes and a standard input/output interface. In fact, Willis teaches or suggests communication between processor nodes, regardless of location, using a message interconnect. Applicants request that the Examiner provide a citation to some reference work recognized as standard in the pertinent art that the elements of claim 26 were conventional and well-known at the time of the application, or withdraw the rejection of claim 26.

CONCLUSION

Therefore, in view of the above remarks this application is in condition for allowance, and the Examiner is respectfully requested to allow this application. The Examiner is invited to contact Applicants' undersigned representative regarding any issues that the Examiner feels are still outstanding.

Respectfully submitted,

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